LISTING OF THE CLAIMS

**CLAIMS**

We claim:

1. (currently amended) An apparatus comprising:

a buffer for storing indications of interrupts generated by a plurality of ports of a peripheral device, ~~the peripheral device having a plurality of ports,~~ said apparatus for transferring interrupts from the peripheral device to a host computer system, and

a controller for, in response to a preset condition being met, generating a control data block comprising a payload portion having a plurality of fields each corresponding to a port from said plurality of ports and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system via one port of the plurality of ports.

2. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that the buffer is full.

3. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed.

4. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed.

5. (Previously presented) An apparatus as claimed in claim 1, wherein the header portion comprises a count indicative of the number of indications included in the payload portion.

6. (original) An apparatus as claimed in claim 1, wherein the header portion comprises a time of day stamp.

7. (original) An apparatus as claimed in claim 1, wherein the buffer comprises a first in - first out memory buffer.

8. (currently amended) A ~~peripheral~~ communications device comprising the apparatus as claimed in claim 1.

9. (currently amended) A data communications network interface comprising the ~~peripheral~~ communications device as claimed in claim 8.

10. (currently amended) An apparatus as claimed in claim 1, further comprising:
a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host ~~computer~~ processing system.

11. (currently amended) A method comprising transferring interrupts from a peripheral device to a host computer system, the peripheral device having a plurality of ports, the ~~step~~ steps of transferring interrupts comprising:

storing interrupts generated by said ports of the peripheral device in a buffer;

determining if a preset condition is met, and, in response to the preset condition being met;

generating a control data block comprising a payload portion having a plurality of fields each corresponding to a different ~~one of the~~ port from said plurality of ports and a header portion having an identifier for identifying the control data block;

moving the contents of the buffer to the corresponding fields of the payload portion; and

sending the control data block to the host computer system via one of the ports.

12. (original) A method as claimed in claim 11, wherein the step of determining if the preset condition is met comprises determining if the buffer is full.

13. (original) A method as claimed in claim 11, wherein the step of determining if the preset condition is met comprises determining if at least a predetermined plurality of indications is stored in the buffer and if a predetermined period has elapsed.

14. (original) A method as claimed in claim 11, wherein the step of determining if the preset condition is met comprises determining if at least one indication is stored in the buffer and if a predetermined period has elapsed.

15. (original) A method as claimed in claim 11, wherein the header portion comprises a count indicative of the number of indications included in the payload portion.

16. (original) A method as claimed in claim 11, wherein the buffer comprises a first in - first out memory buffer.

17. (currently amended) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect ~~the~~ all functions of ~~all the elements~~ the apparatus of claim 1.

18. (currently amended) A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing data processing, the computer readable program code means in said computer program product comprising computer readable program code means for causing a computer to effect ~~the~~ all functions of ~~all the elements~~ the apparatus of claim 10.

19. (currently amended) An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means in said article of manufacture comprising computer readable program code means for causing a computer to effect all ~~the~~ steps ~~and all the limitations of the steps~~ of the method of claim 11.

20. (currently amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for transferring interrupts, said method steps comprising all ~~the~~ steps ~~and all the limitations of the steps~~ of the method of claim 11.

21. (previously presented) An apparatus as claimed in claim 1, wherein:

the preset condition comprises at least one of:

a determination that the buffer is full,

a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed, and

determination that at least one indication is stored in the buffer and that a predetermined period has elapsed;

the header portion comprises a count indicative of the number of indications included in the payload portion;

the header portion comprises a time of day stamp; and

the buffer comprises a first in - first out memory buffer.

22. (currently amended) An apparatus as claimed in claim 21, further comprising:
a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host ~~computer~~ processing system.